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A General Class of Rate-Change Circuits

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Rate changing is encountered in data transmission, distributing, collating, encoding, and decoding. It entails the transformation of data at one rate to data at another predefined rate. It is the object of this paper to investigate a special class of circuits that accomplish such a transformation quite mechanically and methodically when only one clock is available to propagate all the binary bits of information. These circuits can be implemented by magnetic domains, by charge transfer and charge-coupled devices, or by any other technology which permits (i) propagation of binary bits of information by a certain modular "period" or "distance" in a modular unit of time and (ii) gating of preselected bits of information from one branch into one or the other branches of three branch nodes in a circuit. The generalization of rate-changing circuits to distributing, collating, reversing, and reversing-with-rate-changing is also presented in the paper.

1. INTRODUCTION

Algebraic coding schemes[1] increase the length of the information block. Shortened codes[2,3] obtained from such coding schemes further alter the length. When these codes are transmitted uniformly over the telephone networks, a change of rate from the received rate to the transmitted rate is essential. Further, channels carry coded information at different rates. If it is necessary to obtain information at a uniform rate, encode it with a general coding scheme and transmit it over any general channel, decode it to its original rate and refurnish it, then many stages of rate changing are necessary.

To collate bursts of information from many sources onto a signal channel also entails a rate-change process. Distributing circuits which select and uniformly distribute a given number of information bits from longer blocks of uniformly received information are special cases of rate-change circuits. It is the object of this paper to report a set of circuits which perform (*i*) general rate changing, (*ii*) general collating and sorting, and finally (*iii*) reversing and reversing-with-rate-changing

functions. They operate methodically, and mechanically *when only one clock source is available for propagation of information bits.* This condition exists specifically in magnetic domain technology[4,5] with field access propagation and to a less stringent measure in charge-transfer[6] and charge-coupled[7,8] device technologies. In general, the circuits presented can be implemented by any technology that permits (*i*) all binary bits of information to be shifted from one location to the adjoining location within one clock cycle and (*ii*) the channeling of information bits to one or the other branch of a node within a circuit.

For clarity of exposition, the following terms are defined. A "period" is a unit of distance or location by which a binary bit of information may be moved in one unit of time. A "clock cycle" is the smallest unit of time. It is also the time required to propagate one binary bit of information by one period. A "gate" is a device which channelizes a selected number of information bits into one or another branch at a node in a circuit. Such functions can be readily accomplished[5,9,10] in the various technologies[4,6,8] presently under development in the Bell System.

The paper is divided into five sections. After the introduction, Section II describes a general class of rate-change circuits. These circuits become an important element in the collating and distributing circuits described in Section III, and Section IV discusses reversing circuits by which the order of incoming data bits may be reversed. Section V is devoted to conclusions.

II. GENERAL RATE-CHANGE CIRCUITS

The principle of rate changing is explained by two examples in this section. The generality of the principle is proved in Appendix A.

2.1 *Rate-Reducing Circuits*

Example 1. Consider a block of data 8 bits long to be expanded by a ratio of 2, yielding a new rate that is half the original rate. Figure 1 represents a circuit in which the data arrives at the clock rate. The incoming polynomial may be written as

$$u_0 = a_0 + a_1X + a_2X^2 + a_3X^3 + a_4X^4 + a_5X^5 + a_6X^6 + a_7X^7.$$

The four data positions corresponding to the first four terms of u_0 are diverted into the upper part of stage 1 containing N_1 periods, and the second four data positions are diverted in the lower half of stage 1 containing $N_1 + 4$ periods. Gate g_2 diverts the first two data positions into the upper half of stage 2, the next two data positions into the lower

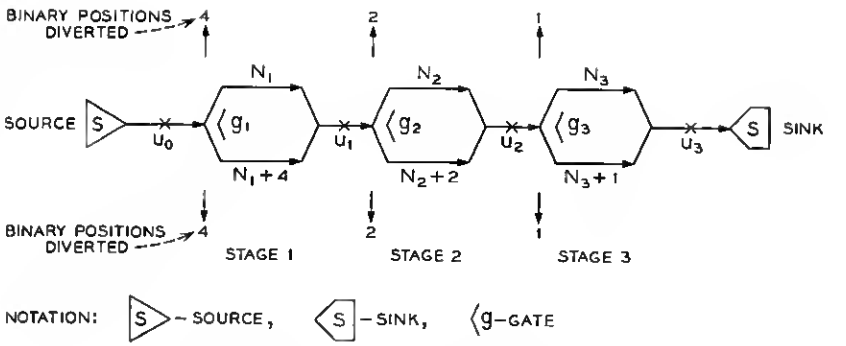

Fig. 1—A simple example of a 2:1 rate-reducing circuit for an 8-bit data block.

half, and so on, so that

$$u_1 = X^{N_1}(a_0 + a_1X + a_2X^2 + a_3X^3) + X^{N_1+4}(a_4X^4 + a_5X^5 + a_6X^6 + a_7X^7)$$

$$= X^{N_1}\{X^0(a_0 + a_1X + a_2X^2 + a_3X^3) + X^8(a_4 + a_5X + a_6X^2 + a_7X^3)\}.$$

Similarly

$$u_2 = X^{N_1}\{X^{N_2}\{X^0(a_0 + a_1X) + X^2(a_2X^2 + a_3X^3) + X^0(a_4X^8 + a_5X^9) + X^2(a_6X^{10} + a_7X^{11})\}$$

$$= X^{N_1+N_2}\{X^0(a_0 + a_1X) + X^4(a_2 + a_3X) + X^8(a_4 + a_5X) + X^{12}(a_6 + a_7X)\}$$

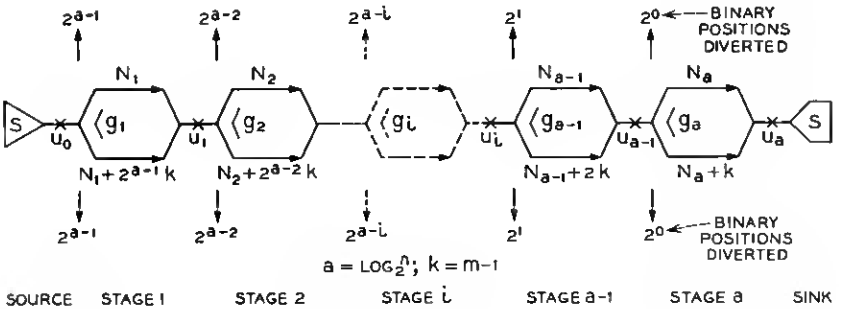

Fig. 1a—General rate-reducing circuit for an n-bit data block and rate ratio of m:1.

and

$$u_3 = X^{N_1+N_2+N_3} \cdot \{a_0 + a_1X^2 + a_2X^4 + a_3X^6 + a_4X^8 + a_5X^{10} + a_6X^{12} + a_7X^{14}\}.$$

The rate of tbe polynomial u_3 corresponds to half the rate of the input polynomial u_0. The output polynomial u_3 has a delay of $(N_1 + N_2 + N_3)$ clock cycles corresponding to the sum of periods in the upper section of the rate-change circuit. In cbarge-transfer and charge-coupled[10] devices $(N_1 + N_2 + N_3)$ can be made zero. In magnetic domain circuits a certain minimum value for $(N_1 + N_2 + N_3)$ is foreseen.

In general it can be seen from Appendix A that the number of stages in a rate-reducing circuit is determined by the number of bit positions in the data block. The differences in periods between the upper half and the lower half of each of the stages are determined by the rate-change ratio. Table I contains the characteristics of a general circuit (Fig. 1a) for an n-bit data stream. The rate-change ratio is m. In Table I, a, denoting the number of stages, is an integer which satisfies the equation

$$2^a \geqq n \quad \text{or} \quad a \geqq \log_2^n, \tag{1}$$

and k is an integer obtained as

$$k = m - 1. \tag{2}$$

The delay in the circuit can be computed as $(N_1 + N_2 + N_3 \cdots N_a)$ clock cycles (see Fig. 1a) from the normal polynomial calculations presented in Appendix A.

2.2 *Rate-Increasing Circuits*

Rate-increasing circuits are derived as inversions of rate-reducing circuits. If the data flow is reversed in a rate-reduction circuit, a rate increase results. The process is investigated in the following example.

Example 2. A block of data 16 bits long, each bit arriving every four clock cycles, is to be condensed to a data block of 16 clock cycles thus

TABLE I—CHARACTERISTICS OF A GENERAL RATE-REDUCING CIRCUIT

Ratio of Input Rate to Output Rate	Number of Bit Positions Diverted by Gates					Difference in Periods in the Stages				
	g_1	g_2	$\cdots$	g_{a-1}	g_a	1	2	—	$a-1$	a
m	2^{a-1}	2^{a-2}	$\cdots$	2^1	2^0	$2^{a-1}k$	$2^{a-1}k$	—	$2k$	k

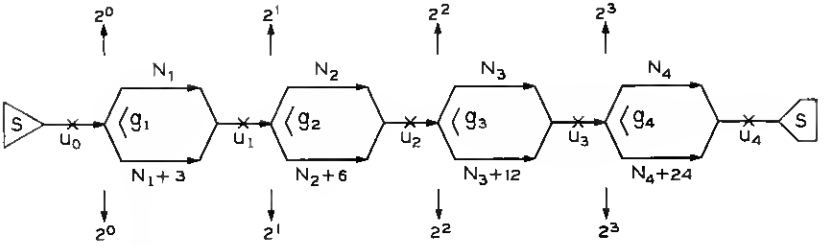

Fig. 2—A 1:4 rate-increasing circuit for a 16-bit data block.

enhancing the rate four times. Figure 2 represents a rate-increasing circuit for the 16-bit data block. The incoming polynomial is

$$u_0 = \sum_{i=0}^{i=15} a_i X^{4i}, \tag{3}$$

and

$$\begin{aligned}
u_1 &= X^{N_1}\{X^3(a_0 + a_1X) + X^{11}(a_2 + a_3X) \\
&\qquad + X^{19}(a_4 + a_5X) + \cdots X^{59}(a_{14} + a_{15}X)\} \\
u_2 &= X^{N_1+N_2}\{X^9(a_0 + a_1X + a_2X^2 + a_3X^3) \\
&\qquad + X^{25}(a_4 + a_5X + a_6X^2 + a_7X^3) + \cdots \\
&\qquad + X^{57}(a_{12} + a_{13}X + a_{14}X^2 + a_{15}X^3)\} \\
u_3 &= X^{N_1+N_2+N_3}\{X^{21}(a_0 + a_1X + \cdots a_7X^7) \\
&\qquad + X^{53}(a_8 + a_9X + a_{10}X^2 \cdots a_{15}X^7)\} \\
u_4 &= X^{N_1+N_2+N_3+N_4}\{X^{45}(a_0 + a_1X + a_2X^2 \cdots a_{15}X^{15})\}.
\end{aligned} \tag{4}$$

The X^{45} term indicates the delay for the first bit which passes through the extra

$$(3 + 6 + 12 + 24) = (m - 1) \sum_{0}^{a-1} 2^i$$

periods corresponding to the four stages of the rate-change circuit. (See also Appendix B.) Table II shows a circuit characteristic for an n-bit data stream where the rate change is $1:m$. The polynomial calculations are presented in Appendix B. When it is desired to change the rate by a fraction $(m_1:m_2)$, a combination of rate-increasing and rate-decreasing circuits may be used in series. It is then necessary to choose the main clock frequency (f_c) which corresponds to the lowest multiple of m_1, m_2, and the incoming data frequency (f_{in}). The first section of

the combined circuit will enhance the frequency from f_{in} to f_c, and the second section will reduce from f_c to the desired frequency of $f_{in}m_2/m_1$. For instance if the input rate is 2400 baud and it is desired to obtain 3600 baud, then a clock rate of 7200 cycles per second will be necessary. The entire circuit for this example is shown in Fig. 3 for a data block 32 bits long.

2.3 *Fractional Ratio Rate-Changing Circuits*

It is sometimes possible to combine the two independent circuits into one circuit and accomplish fractional ratio rate changing. It becomes necessary however to perform a special function of delaying selected bit positions by a fractional cycle. An example of this circuit is presented for a 2:3 rate-change circuit.

Example 3. A block of data 8 bits long wbich arrives uniformly during 12 clock cycles is to be condensed to a data block of 8 clock cycles. The incoming data polynomial u_0 in Fig. 3a is

$$u_0 = a_0X^0 + a_1X^{3/2} + a_2X^3 + a_3X^{9/2} + a_4X^6 + a_5X^{15/2} + a_6X^9 + a_7X^{21/2}. \quad (5)$$

The polynomial u_1 after delaying alternate bit positions by half a cycle is

$$u_1 = X^{1/2}\{(a_0 + a_1X) + X^3(a_2 + a_3X) + X^6(a_4 + a_5X) + X^9(a_6 + a_7X)\}. \quad (6)$$

After the first stage of the circuit in which the gate g_1 diverts the two data positions for tbree clock cycles into the lower balf of the stage and the two data positions for the next three cycles into the top half of the stage, the polynomial u_2 may be written as

$$\begin{aligned} u_2 &= X^{1/2}\{X^{N_1+1}(a_0 + a_1X) + X^{N_1}(X^3(a_2 + a_3X)) \\ &\quad + X^{N_1+1}(X^6(a_4 + a_5X)) + X^{N_1}(X^9(a_6 + a_7X))\} \\ &= X^{N_1+3/2}\{(a_0 + a_1X + a_2X^2 + a_3X^3) + X^6(a_4 + a_5X + a_6X^2 + a_7X^3)\}, \end{aligned} \quad (7)$$

TABLE II—CHARACTERISTICS OF A GENERAL RATE-INCREASING CIRCUIT

Ratio of Input Rate to Output Rate	Number of Bit Positions Diverted by Gates					Difference in Periods in the Stages				
	g_1	g_2	g_3	$\cdots$	g^a	1	2	—	$a-1$	a
$1:m$	2^0	2^1	2^2	$\cdots$	2^{a-1}	k	$2k$	—	$2^{a-2}k$	$2^{a-1}k$

and similarly

$$u_3 = X^{N_1+3/2}\{X^{N_2+2}(a_0 + a_1X + a_2X^2 + a_3X^3) + X^{N_2+6}(a_4 + a_5X + a_6X^2 + a_7X^3)\}$$

$$= X^{N_1+N_2+7/2}\{a_0 + a_1X + a_2X^2 + a_3X^3 + a_4X^4 + a_5X^5 + a_6X^6 + a_7X^7\}. \quad (8)$$

The magnetic domain technology is especially suitable for creating an effect obtained by delaying the alternate bit position by half a clock cycle. The peculiarities of the T-bar circuits[4] may be exploited in achieving this effect. Figure 3b shows two generators, G_1 and G_2, excited by the same generating current in the coil. The "seed bubbles" (see Ref. 4) of both the generators rotate with the main driving field in synchronism. When the coil is excited every 3/2 cycles, G_1 and G_2 generate bubbles corresponding to the alternate binary bits. The distance between the bubbles in section A or section B of the circuit will be three T-bar periods. At the junction of A and B, the effect of the split Tee will add a quarter period (i.e., $X^{1/4}$) for the bubbles in section B and subtract a quarter period (i.e., $X^{-1/4}$) for bubbles in section A, and the net effect will be to delay the alternate bubble position by half a cycle ($X^{1/2}$). The polynomial in section C of the circuit will already have a form identical to u_1 in (6).

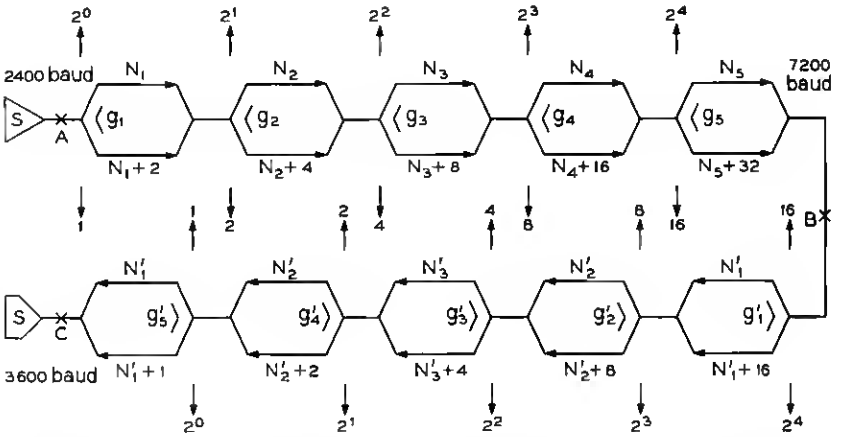

Fig. 3—An example of combination rate-reducing and rate-increasing circuits for a 2:3 rate-change circuit for a data block 32 bits long.

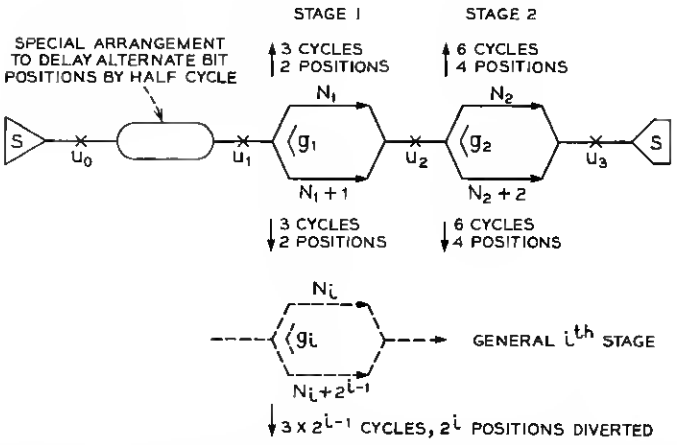

Fig. 3a—A circuit arrangement for a 2:3 ratio rate change for an 8-bit data stream. It is possible to add more stages for longer data streams.

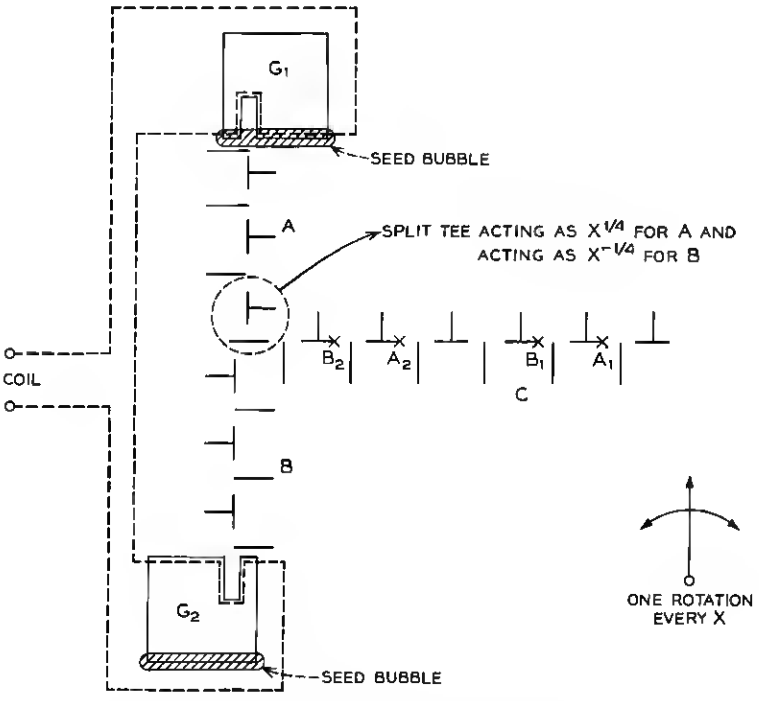

Fig. 3b—Two generators, G_1 and G_2, excited by the same coil, generate alternate bit positions; i.e., G_1 generates a_0, a_2, a_4—and G_2 generates a_1, a_3, a_5—.

III. COLLATING AND DISTRIBUTING CIRCUITS

To avoid undue complications in the polynomial algebra, one example of collating circuit and one example of distributing circuit are presented in this section. It is possible to generalize the polynomial calculations for any general incoming polynomial u_0.

Example 4. Four 4-bit inputs from channels 1, 2, 3, and 4 are to be collated onto one channel (see Fig. 4). Let the incoming polynomials be

$$u_1 = a_0X^0 + a_1X + a_2X^2 + a_3X^3,$$
$$u_2 = a_4X^4 + a_5X^5 + a_6X^6 + a_7X^7,$$
$$u_3 = a_8X^8 + a_9X^9 + a_{10}X^{10} + a_{11}X^{11},$$

and

$$u_4 = a_{12}X^{12} + a_{13}X^{13} + a_{14}X^{14} + a_{15}X^{15}, \tag{9}$$

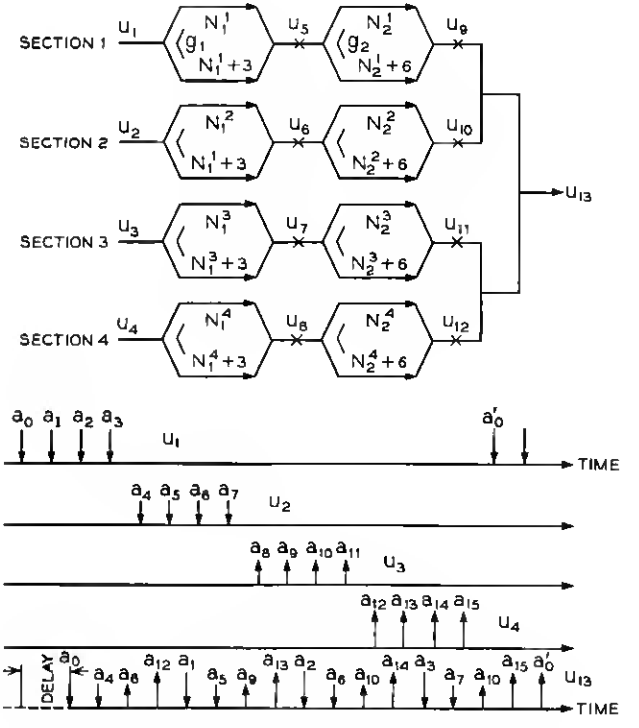

Fig. 4—A typical 4-input, 4-bit collating circuit.

then each of the sections 1, 2, 3, and 4 must accomplish a rate reduction of 1:4. Let

N_1^1 and N_2^1 be the number of periods in top sections of 1,
N_1^2 and N_2^2 be the number of periods in top sections of 2,
N_1^3 and N_2^3 be the number of periods in top sections of 3, and
N_1^4 and N_2^4 be the number of periods in top sections of 4.

According to Section II, the lower halves of sections 1, 2, 3, and 4 are $(N_1^1 + 3)$, $(N_2^1 + 6)$, and so on. The polynomial u_5 between the two stages of the first section is

$$u_5 = X^{N_1^1}\{(a_0 + a_2X^2) + X^4(a_1 + a_3X^2)\}, \tag{10}$$

and so on. The polynomials u_9, u_{10}, u_{11}, and u_{12} may be calculated as

$$\begin{aligned}
u_9 &= X^{N_1^1+N_1^2}\{a_0 + a_1X^4 + a_2X^8 + a_3X^{12}\} \\
u_{10} &= X^{N_1^2+N_1^3+4}\{a_4 + a_5X^4 + a_6X^8 + a_7X^{12}\} \\
u_{11} &= X^{N_1^3+N_1^4+8}\{a_8 + a_9X^4 + a_{10}X^8 + a_{11}X^{12}\} \\
u_{12} &= X^{N_1^4+N_2^4+12}\{a_{12} + a_{13}X^4 + a_{14}X^8 + a_{15}X^{12}\}.
\end{aligned} \tag{11}$$

The periods in sections 1, 2, 3, and 4 are chosen such that

$$\begin{aligned}
N_1^1 + N_2^1 &= N_1^4 + N_2^4 + 9 \\
N_2^2 + N_2^2 &= N_1^4 + N_2^4 + 10 \\
N_3^2 + N_2^3 &= N_1^4 + N_2^4 + 11.
\end{aligned} \tag{12}$$

If the technology for implementation permits $N_1^4 + N_2^4 = 0$, then

$$\begin{aligned}
u_9 &= X^9(a_0 + a_1X^4 + a_2X^8 + a_3X^{12}) \\
u_{10} &= X^{10}(a_4 + a_5X^4 + a_6X^8 + a_7X^{12}) \\
u_{11} &= X^{11}(a_8 + a_9X^4 + a_{10}X^8 + 9_{11}X^{12}) \\
u_{12} &= X^{12}(a_{12} + a_{13}X^4 + a_{14}X^8 + a_{15}X^{12}).
\end{aligned} \tag{13}$$

The output polynomial u_{13} can be written as:

$$\begin{aligned}
u_{13} = X^9\{&a_0 + a_4X + a_8X^2 + a_{12}X^3 \\
&+ a_1X^4 + a_5X^5 + a_9X^6 + a_{13}X^7 \\
&+ a_2X^8 + a_6X^9 + a_{10}X^{10} + a_{14}X^{11} \\
&+ a_3X^{12} + a_7X^{13} + a_{11}X^{14} + a_{15}X^{15}\};
\end{aligned} \tag{14}$$

and X^9 corresponds to the minimum delay in the circuit. It can be seen

that $N_1^4 + N_2^4$ need not equal zero. However, equations (12) must be satisfied. Under these conditions a fixed delay between the input and output results. Further, it is to be noted that equations (12) must be chosen with care to ascertain that the output polynomial u_{13} has each of its term a_bX^c satisfying the equation

$$(\text{minimum delay}) + c \geqq b \tag{15}$$

where b is the power of X in any one of the terms a_bX^b in the input polynomial. Physically relation (15) implies that no term in the output appears before it has been received at the input terminal. In equations (12), as b varies between 0 and 15, the corresponding values of c in equation (14) satisfy relation (15).

Other generalizations of this circuit can be readily obtained by changing the number of stages (depending upon the number of bits in u_1 , u_2 $\cdots$ etc.) and the number of inputs to be collated. Reversing the direction of propagation yields a reversal of input and output polynomials leading to the distributing circuit.

Example 5. A typical distributing circuit is shown in Fig. 5. The input polynomial is

$$u_0 = a_0X^0 + a_1X + a_2X^2 \cdots a_{15}X^{15}. \tag{16}$$

The binding conditions on this circuit imply that

$$N_1^1 + N_2^1 + N_3^1 = N_1 + N_2 + N_3 + 7.* \tag{17}$$

The polynomial calculations lead to the output polynomial

$$\begin{aligned} u_7 = X^7\{&a_0 + a_2X + a_4X^2 + a_6X^3 + a_8X^4 + a_{10}X^5 + a_{12}X^6 + a_{14}X^7 \\ &+ a_1X^8 + a_3X^9 + a_5X^{10} + a_7X^{11} + a_9X^{12} + a_{11}X^{13} \\ &+ a_{13}X^{14} + a_{15}X^{15}\}. \end{aligned} \tag{18}$$

It can be seen that if the direction of propagation is reversed, the circuit performs a collating function.

IV. REVERSING CIRCUITS

These circuits are capable of changing the order of data bits in an incoming polynomial. If the input polynomial is $u_0 = \sum_0^n a_iX_i$ then the output of the circuit can be written as $u_a = X^d \sum_0^n a_{n-i}X^i$. To

* Alternatively the lower half of the entire circuit may be designed to have seven additional periods if

$$N_1^1 + N_2^1 + N_3^1 = N_1 + N_2 + N_3 .$$

Under these conditions the gating at g_2 , g_3 , and g_4 is somewhat simplified.

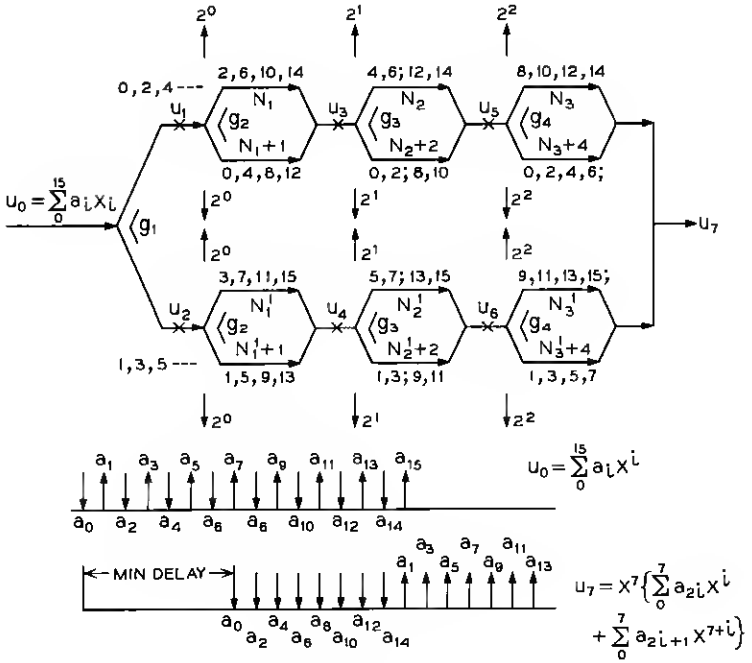

Fig. 5—An example of a distributing circuit.

satisfy the physical constraint that no term of the output polynomial appears at the output before it is received at the input

$$d \geqq n. \tag{19}$$

A specific example of reversing an 8-bit data block is presented in this section. The generality of this type of circuit is proved in Appendix C.

Example 6. It is desired to reverse an 8-bit data block represented as

$$u_0 = a_0X^0 + a_1X + a_2X^2 + a_3X^3 + a_4X^4 + a_5X^5 + a_6X^6 + a_7X^7. \tag{20}$$

After this data block is processed by the first stage in the circuit (Fig. 6)

$$u_1 = X^{N_1}\{X(a_1 + a_0X) + X^3(a_3 + a_2X) + X^5(a_5 + a_4X) + X^7(a_7 + a_6X)\}.$$

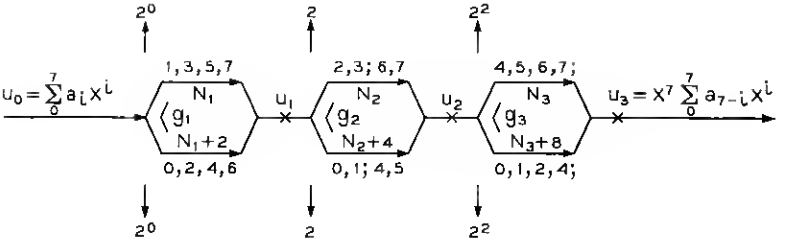

Fig. 6—An example of a reversing circuit (the general reversing circuits are presented in Figs. 8 and 9).

Further, u_2 and u_3 can be written as

$$u_2 = X^{N_1+N_2}\{X^3(a_3 + a_2X + a_1X^2 + a_0X^3) + X^7(a_7 + a_6X + a_5X^2 + a_4X^3)\}$$

$$u_3 = X^{N_1+N_2+N_3}\{X^7(a_7 + a_6X + a_5X^2 + a_4X^3 + a_3X^4 + a_2X^5 + a_1X^6 + a_0X^7)\}.$$

If the technology for implementation permits $N_1 + N_2 + N_3 = 0$, then

$$u_3 = X^7\{a_7 + a_6X + a_5X^2 + a_4X^3 + a_3X^4 + a_2X^5 + a_1X^6 + a_0X^7\}. \quad (21)$$

V. CONCLUSIONS

The techniques presented in this paper indicate simple combinations of gating and propagation functions to yield any general rate-changing, collating, distributing, and reversing of data streams. All tbe necessary gates are generally driven by one binary clock diverting 2^0, 2, 2^2, $\cdots$ binary position (or "domains") from one branch into one or the other branches of three branch nodes distributed systematically in the circuit. Further, the circuit configurations are optimal within the constraints of the problem to the extent that a minimum number of gates are necessary to accomplish any one of the rate changing, distributing, collating, or reversing functions. For this general reason the control circuitry necessary for implementation of these configurations is reduced to a minimum.

Bubble technology, charge-transfer, or charge-coupled device technology each lends itself to the implementation of such circuits.

APPENDIX A

Generalized Calculation for a Rate-Decreasing Circuit

Let m be the ratio of the incoming data rate to the desired rate and n be the number of data bits in the data stream. For initial calculations let us choose n to be 2^a where a is an integer. The incoming polynomial can be represented as

$$u_0 = a_0X^0 + a_1X + a_2X^2 + a_3X^3 + \cdots a_{n-1}X^{n-1}.$$

After the first stage of the general circuit shown in Fig. 1a,

$$u_1 = X^{N_1}[X^0\{a_0X^0 + a_1X \cdots a_{n'-1}X^{n'-1}\} + X^{nk}\{a_{n'}X^{n'} + \cdots a_{n-1}X^{n-1}\}$$

where $n' = 2^{a-1}$ and $k = m - 1$. Or u_1 can be written as

$$u_1 = X^{N_1}\{X^0(a_0X^0 + a_1X + \cdots a_{n'-1}X^{n'-1}) + X^{n'(k+1)}(a_{n'}X^0 + a_{n'+1}X + \cdots a_{n-1}X^{n'-1})\}.$$

After the second stage of the general circuit

$$u_2 = X^{N_1+N_2}\{X_0(a_0X^0 + a_1X \cdots a_{n'-1}X^{n''-1}) + X^{n''(k+1)}\{a_{n''}X^0 + \cdots a_{n'-1}X^{n''-1}\} + X^{n'(k+1)}(a_{n'}X^0 + \cdots a_{n'+n''-1}X^{n''-1}) + X^{(n''+n')(k+1)}(a_{n'+n''}X^0 \cdots a_{n-1}X^{n''-1})\}$$

where $n'' = 2^{a-2}$.

After the $(a - 1)$st stage

$$u_{a-1} = X^{N_1+N_2\ldots N_{a-1}}\{X_0(a_0X^0 + a_1X) + X^{2m}(a_2 + a_3X) \cdots X^{(n-2)m}(a_{n-2} + a_{n-1}X)\}$$

and after the ath stage

$$u_a = X^{\sum_1^a N_i}\{aX^0 + a_1X^m + a_2X^{2m} + a_3X^{3m} \cdots a_{n-2}X^{(n-2)m} + a_{n-1}X^{m(n-1)}\}$$

since $m = k + 1$ and $a = \log_2^n$. It can be seen that the rate for the u_a polynomial is $(1/m)$th the rate of the incoming polynomial u_0. When the number of data bits n does not equal a number 2^a, the general polynomial calculations become more complicated, but the difference

of elements in the two branches is still the same, and the gates can still be driven by binary counters. When the circuit is used on a repetitive basis, the gating sequence of the various gates g_1, g_2 $\cdots$ g_a must be altered to adjust for the value of n. One such sequence of a gate operation for a 26-bit, 2:1 rate-decreasing circuit (shown in Fig. 7) is presented in Table III.

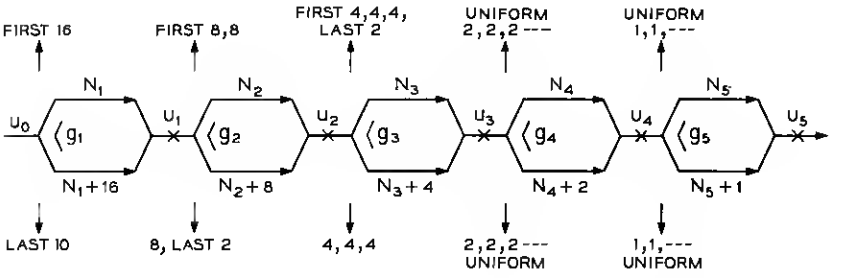

Fig. 7—A typical 2:1 rate-decreasing circuit for a 26-bit data block.

APPENDIX B

Generalized Calculation for a Rate-Increasing Circuit

Let m be the rate increase desired and n be the number of bits in the data stream. For initial calculation let us choose n as a 2^a where a is an integer. The incoming data polynomial may be written as

$$u_0 = a_0X^0 + a_1X^m + a_2X^{2m} + a_3X^{3m} \cdots a_{n-1}X^{(n-1)m}.$$

After the first stage of the general rate-increasing circuit (Fig. 8),

$$u_1 = X^{N_1}\{X^{m-1}(a_0 + a_1X) + X^{3m-1}(a_2 + a_3X) \cdots a^{(n-1)m-1}(a_{n-2} + a_{n-1}X)\}.$$

TABLE III—SEQUENCE OF GATE OPERATION FOR A 26-BIT DATA STREAM

Number of Bit Positions Diverted by Gates				Difference in Periods in Different Stages					
g_1	g_2	g_3	g_4	g_5	1	2	3	4	5
16, 10;	; 8, 8, 8, 2;	; 4, 4, 4, 4, 4, 4, 2;	; 2, 2, ... 2, 2;	;1, 1, ... 1, 1;	16	8	4	2	1

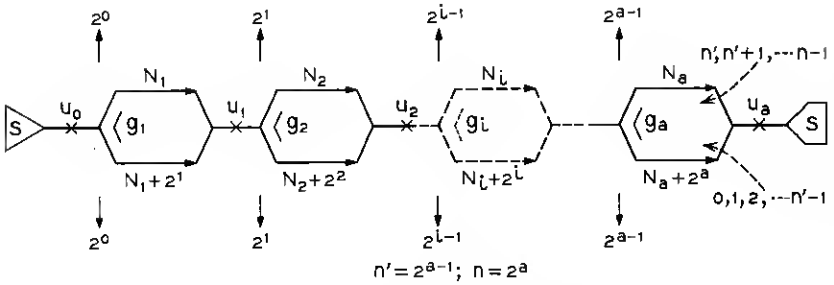

Fig. 8—A general reversing circuit for an n-bit data block.

After the second stage

$$u_2 = X^{N_1+N_2}\{X^{3m-3}(a_0 + a_1X + a_2X^2 + a_3X^3) + \cdots + X^{(n-1)m-3}(a_{n-4} + a_{n-3}X + a_{n-2}X^2 + a_{n-1}X^3)$$

$$= X^{\sum_1^2 N_i}\{X^{\sum_0^1 2^i(m-1)}(a_0 + a_1X + a_2X^2 + a_3X^3) + \cdots + X^{(n-1)m-\sum_0^1 2^i(m-1)}(a_{n-4} + a_{n-3}X + a_{n-2}X^2 + a_{n-1}X^3)\}.$$

After the ath stage,

$$u_a = X^{\sum_1^a N_i}\{X^{\sum_0^{a-1} 2^i(m-1)}(a_0 + a_1X + a_2X^2 + \cdots a_{n-1}X^{n-1})\}.$$

When it is necessary to cover the case in which n is not 2^a but any given number, it is essential to choose an integer number, a, such that

$$2^a \geqq n.$$

The functioning of the rate-increasing circuit can be proved in the following way:

The power of X associated with any term a_i in the converted polynomial u_a can be written as the delay d' which the circuit introduces and

$$d' = \sum_{j=0}^{j=a-1} 2^j(m-1) + i.$$

(See tbe expression for u_a in this appendix and assume $\sum_1^a N_i = 0$). The first term a_0 of the incoming polynomial u_0 must be delayed by $((n-1)m - (n-1))$ clock cycles to ascertain tbat a_0 is $(n-1)$ clock cycles ahead of a_{n-1} , the last term in u_0 . After the conversion to u_a the ith term will have to be i clock cycles behind a_0 in u_a . This leads to the total delay d'' for ith term as

$$d'' = ((n-1)m - (n-1)) + i \quad \text{clock cycles}$$

$$= (n - 1)(m - 1) + i$$
$$= (2^a - 1)(m - 1) + i$$
$$= \sum_{i=0}^{i=a-1} 2^i(m - 1) + i.$$

This corresponds to the delay d' in the polynomial u_a.

APPENDIX C

Generalized Calculation for a Reversing Circuit

Consider a block of binary data with n-bit positions and a reversing circuit shown in Fig. 8. To simplify the nature of equations let us assume that $n = 2^a$ where a is an integer. This constraint can, however, be easily relaxed in practice as shown in Appendix A

$$u_0 = a_0X^0 + a_1X^1 + a_2X^2 \cdots a_{n-1}X^{n-1}$$
$$u_1 = X^{N_1}\{(a_0X^2 + a_1X) + (a_2X^4 + a_3X^3) + \cdots a_{n-2}X^{n+1} + a_{n-1}X^{n-1}\}$$
$$u_1 = X^{N_1}\{X(a_1 + a_0X) + X^3(a_3 + a_2X) + \cdots X^{n-1}(a_{n-1} + a_{n-2}X)\}.$$

Similarly

$$u_{a-1} = X^{\sum_1^{a-1} N_i}\{X^{n'-1}(a_{n'-1} + a_{n'-2}X \cdots a_0X^{n'-1}) + X^{n-1}(a_{n-1} + a_{n-2}X \cdots a_{n-n'}X^{n'-1})\}$$

where $n' = 2^{a-1}$; $n' = n/2$ and finally

$$u_a = X^{\sum_1^a N_i}\{X^{n-1}(a_{n-1} + a_{n-2}X + a_{n-3}X^2 \cdots a_0X^{n-1})\}.$$

The order of the polynomial u_0 is reversed. The minimum delay that is essential in the circuit is $(n - 1)$ cycles to satisfy the physical constraint that a_{n-1} appear at the output only after it is received hy the circuit. The delay of $\sum_1^a N_i$ depends on the nature of the basic vehicle for implementation. With magnetic domain circuits a certain minimum is deemed necessary. With charge-transfer or charge-coupled devices the value can he made zero.

When a rate change and reversing are both desired, the number of periods in the lower section of any stage i should become

$$(N_i + a^i + a^{i-1} \cdot k)$$

where $k = m - 1$ and m is the rate change desired. The general circuit for a comhination reversing-rate change circuit is shown in Fig. 9. The

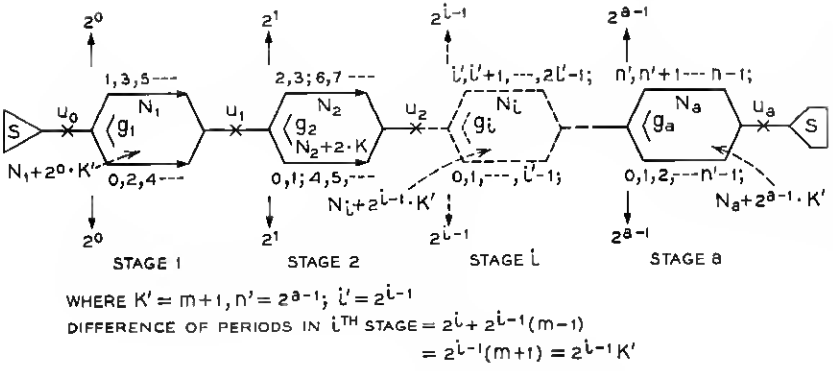

Fig. 9—A combined reversing and 1:m rate-change circuit.

polynomial calculations are very similar to those presented in Appendixes A and B.

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